REMARKS/ARGUMENTS

The Examiner is thanked for the clarity and conciseness of the previous Office Action, and for the citation of references, which have been studied with interest and care.

This Amendment is in response to the Office Action mailed March 22, 2005. In the Office Action, claims 1-5, 8-15, and 18-27 stand rejected under 35 U.S.C. § 102, and claims 6, 7, 16, 17, and 28-38 stand rejected under 35 U.S.C. § 103.

Applicant has amended independent claims 1, 12, 20, and 28 to clarify embodiments of the invention.

Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 102

Claims 1-5, 8-15, and 18-27 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent No. 5,790,130 issued to Gannett (hereinafter Gannett).

Applicant has re-written the dependent features of dependent claims 3, 14, 22, and 30 into amended independent claims 1, 12, 20, and 28, to further clarify embodiments of the invention. Applicant respectfully submits that amended independent claims 1, 12, 20, and 28 are neither anticipated nor rendered obvious by Gannett.

As to anticipation, as set forth in the MPEP § 2131, anticipation requires:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). ... "The *identical invention* must be shown in as complete detail as contained in the ... claim." (Emphasis added). *Richardson v. Suzuki Motor Co., 868* F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

Utilizing amended independent claim 1 as an example, Applicant's amended independent claims 1, 12, 20, and 28 generally recite an image signal processor comprising: a local memory to store data...*a memory command handler including a plurality of memory address generators*, each memory address generator to generate a memory address to a local memory and to interpret a command to be performed on the data of the local memory located at the memory address to aid in image processing tasks...and...*a plurality of cluster communication registers coupled to the plurality of the memory address generators, the plurality of cluster communication registers storing data to be sent to the local memory and commands to be performed by the memory address generator.*

Applicant respectfully submits that Gannett is directed towards a different invention and does not teach or suggest the limitations of Applicant's amended independent claims.

Although, as pointed out by the previous Office Action, Gannett does disclose in Figure 3, a hardware device 150 having a local memory 155 to implement image processing, other than that, the limitations of Applicant's amended independent claims are not taught or suggested by Gannett.

To begin with, the Office Action utilizes texture interrupt managing daemons (TIMs)170, 172, and 174 of Figure 3A as allegedly teaching Applicant's memory command handler.

Applicant respectfully submits that these texture interrupt managing daemons (TIMs) do not teach or suggest Applicant's limitations related to a *memory command handler* including a plurality of memory address generators in which each memory address generator generates a memory address to the local memory and interprets a command to be performed on the data of the local memory located at the memory address to aid in image processing tasks.

Instead, as set forth in column 8, lines 50-54 of Gannett:

"The invention relates to a texture interrupt managing daemon (TIM) 150 that is an independent, stand alone software process that runs on the processor of the host computer, unbeknownst to the user...The TIM 160 of the present invention communicates with each of the graphics hardware drivers over a distinct socket..."

Thus, the TIMs of Gannett are independent stand alone software processes that run on the processor and are independent of the image processor of Gannett, i.e., the hardware device 150. Thus, these TIMs are not part of the image processor hardware. Instead, the TIM 160, 170, 172, 174 are located outside and are distinct from the respective graphic hardware devices 150, 164, 166, and 168 and are in fact software processes.

This is in stark contrast to Applicant's claim limitations related to a hardware-based memory command handler located within the image processor itself.

Moreover, Applicant respectfully submits that nowhere does Gannett teach or suggest: *a plurality of cluster communication registers coupled to the plurality of the memory address generators...the plurality of cluster communication registers storing data to be sent to the local memory and commands to be performed by the memory address generators.*

Although the previous Office Action cited column 16, lines 22-23 of Gannett as being relevant to this limitation, Applicant respectfully submits that Gannett does not teach or suggest this limitation in combination with Applicant's other claim limitations.

Particularly, column 16, lines 22-23 of Gannett states "The pipeline interface includes a set of master registers and a set of corresponding slave registers."

More particularly, column 16, lines 15-30, of Gannett states that: "[T]he texture mapping chip 46 is shown in Figure 5…The chip 46 includes a front-end pipeline interface 60 that receives object and texture primitive data from the front-end board over 64-bit bus 18…The pipeline interface includes a set of master registers and a set of corresponding slave registers…During rendering, the master registers are filled sequentially with fifty-two digital words of data that define the primitive…Then, upon receipt of an appropriate rendering command, the data is shifted into slave registers in the pipeline interface, allowing, in a pipelined fashion the master registers to be filled with the data representing another primitive…"

Thus, Applicant respectfully submits that Gannett's pipeline interface utilizing master and slave registers for pipelining is completely different and does not teach or suggest Applicant's *plurality of cluster communication registers coupled to the plurality of memory*

address generators within an image processor wherein the plurality of cluster communication registers store data to be sent to local memory and commands to be performed by the memory address generators.

Applicant respectfully submits that it is quite clear that Gannett does not teach or suggest Applicant's amended independent claim limitations of amended independent claims 1, 12, 20, and 28 and Applicant respectfully submits that these claims should be allowed and passed to issuance. Further, Applicant respectfully submits that the dependent claims therefrom also be allowed and passed to issuance.

Conclusion

In view of the remarks made above, it is respectfully submitted that pending claims 1, 4-12, 15-20, 23-28, and 31-38 define the subject invention over the prior art of record. Thus, Applicant respectfully submits that all the pending claims are in condition for allowance, and such action is earnestly solicited at the earliest possible date. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application. To the extent necessary, a petition for an extension of time under 37 C.F.R. is hereby made. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such account.

Respectfully submitted,

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Dated: 5/19/2005

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Nicole Erquiaga *Date*